CLAIMS

I/We claim:

[c1] 1. A method for packaging microelectronic substrates, comprising:

positioning a first microelectronic substrate proximate to a second microelectronic substrate, the first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface, the second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface;

coupling the first microelectronic substrate to the second microelectronic substrate to form a substrate assembly with the first surface of the first microelectronic substrate facing toward the second surface of the second microelectronic substrate; and

sequentially disposing at least first and second portions of a conductive material on the substrate assembly to build up a conductive structure connected between the first connection site of the first microelectronic substrate and the second connection site of the second microelectronic substrate.

[c2] 2. The method of claim 1, further comprising:

disposing a first portion of dielectric material on the first microelectronic substrate;

disposing a second portion of dielectric material on the second microelectronic substrate; and

conforming the conductive material to the first and second portions of dielectric material.

[c3] 3. The method of claim 1, further comprising:

disposing a first portion of dielectric material on the first microelectronic substrate;

stacking the second microelectronic substrate on the first microelectronic substrate;

disposing a second portion of dielectric material on the second microelectronic substrate;

conforming the conductive material to the first and second portions of dielectric material;

disposing a third portion of dielectric material on the conductive material;

coupling a third connection site to the conductive material with the third connection site electrically coupled to the first and second connection sites; and

disposing a volume of flowable conductive material on the third connection site to provide electrical communication with the first and second microelectronic substrates.

[c4] 4. The method of claim 1, further comprising positioning the first and second microelectronic substrates with the first and second connection sites facing in at least approximately the same direction.

[c5] 5. The method of claim 1 wherein the first microelectronic substrate is one of a plurality of first microelectronic substrates, the second microelectronic substrate is one a plurality of second microelectronic substrates, and the connection structure is one of a plurality of connection structures, and wherein the method further comprises:

while the first microelectronic substrates are attached to each other to define at least a portion of a microelectronic wafer, coupling each of the plurality of second microelectronic substrates to a corresponding

one of the plurality of first microelectronic substrates to form a plurality of substrate assemblies;

for each substrate assembly, sequentially disposing portions of the conductive material to build up one of the conductive structures connected between the first and second connection sites of each substrate assembly; and

separating the substrate assemblies from each other.

[c6] 6. The method of claim 1, further comprising electrically coupling the substrate assembly to a microelectronic device external to the assembly while at least one edge of the first microelectronic substrate is exposed.

[c7] 7. The method of claim 1, further comprising disposing a dielectric material on the first microelectronic substrate and conforming the conductive structure to a contour of the dielectric material.

[c8] 8. The method of claim 1, further comprising:

selecting the first microelectronic substrate to have a first planform area in the plane of the second surface of the first microelectronic substrate; and

selecting the second microelectronic substrate to have a second planform area in the plane of the second surface of the second microelectronic substrate, with the second planform area less than the first planform area.

[c9] 9. The method of claim 1, further comprising disposing a dielectric material between the first surface of the first microelectronic substrate and the second surface of the second microelectronic substrate and coupling the first and second microelectronic substrates to each other by adhering the first and second microelectronic substrates to the dielectric material.

[c10] 10. The method of claim 1 wherein coupling the first and second microelectronic substrates includes connecting the first and second microelectronic substrates to an intermediate structure.

[c11] 11. The method of claim 1, further comprising disposing an adhesive film on the second microelectronic substrate and contacting the adhesive film with the first microelectronic substrate to adhere the second microelectronic substrate to the first microelectronic substrate.

[c12] 12. The method of claim 1 wherein disposing the conductive material includes disposing the conductive material to form an elongated conductive structure that extends in three orthogonal directions between the first and second connection sites.

[c13] 13. The method of claim 1 wherein disposing the conductive material includes disposing a non-self-supporting conductive material between the first and second connection sites.

[c14] 14. The method of claim 1 wherein disposing the conductive material includes depositing the conductive material by sputtering, chemical vapor deposition or physical vapor deposition.

[c15] 15. The method of claim 1, further comprising selecting the first microelectronic substrate to include an SRAM device and selecting the second microelectronic substrate to include a flash memory device.

[c16] 16. The method of claim 1 wherein the conductive material is a first conductive material, and wherein the method further comprises:

coupling a third microelectronic substrate to the second microelectronic substrate, the third microelectronic substrate having a first surface

with a third connection site, the third microelectronic substrate further having a second surface facing opposite the first surface, the second surface of the third microelectronic substrate facing toward the first surface of second microelectronic substrate; and

sequentially disposing first and second portions of a second conductive material on the substrate assembly to extend the conductive structure connected between the third connection site of the third microelectronic substrate and the second connection site of the second microelectronic substrate.

[c17] 17. A method for packaging microelectronic substrates, comprising:

positioning a first microelectronic substrate proximate to a second microelectronic substrate, the first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface, the second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface;

coupling the first microelectronic substrate to the second microelectronic substrate to form a substrate assembly with the first surface of the first microelectronic substrate facing toward the second surface of the second microelectronic substrate; and

electrically connecting the first and second connection sites by disposing a conductive material on the substrate assembly between the first and second connection sites and conforming the conductive material at least generally to a contour of the substrate assembly immediately adjacent to the conductive material.

[c18] 18. The method of claim 17 wherein coupling the first and second microelectronic substrates includes coupling the first and second microelectronic

substrates with the first and second connection sites facing in at least approximately the same direction.

[c19] 19. The method of claim 17 wherein electrically connecting the first and second connection sites includes conforming the conductive material to a contour defined by a dielectric material on the first surface of at least one of the first and second microelectronic substrates.

[c20] 20. The method of claim 17, further comprising disposing at least one dielectric material on the first and second microelectronic substrates to form a first layer portion adjacent to the first microelectronic substrate and a second layer portion adjacent to the second microelectronic substrate, and conforming the conductive material to the first and second layer portions.

[c21] 21. The method of claim 17, further comprising disposing a generally non-conductive material on the second surface of the first microelectronic substrate.

[c22] 22. The method of claim 17 wherein disposing the conductive material includes sequentially disposing at least first and second portions of the conductive material on the substrate assembly to build up a conductive structure connected between the first connection site of the first microelectronic substrate and the second connection site of the second microelectronic substrate.

[c23] 23. The method of claim 17, further comprising:

disposing a first portion of dielectric material on the first microelectronic substrate;

stacking the second microelectronic substrate on the first microelectronic substrate;

disposing a second portion of dielectric material on the second microelectronic substrate;

conforming the conductive material to the first and second portions of dielectric material;

disposing a third portion of dielectric material on the conductive material;

coupling a third connection site to the conductive material with the third connection site electrically coupled to the first and second connection sites; and

disposing a volume of flowable conductive material on the third connection site to provide electrical communication with the first and second microelectronic substrates.

[c24] 24. The method of claim 17 wherein the first microelectronic substrate includes one of a plurality of first microelectronic substrates, the second microelectronic substrate includes one a plurality of second microelectronic substrates, and the connection structure is one of a plurality of connection structures, and wherein the method further comprises:

while the first microelectronic substrates are attached to each other to define at least a portion of a microelectronic wafer, coupling each of the plurality of second microelectronic substrates to a corresponding one of the plurality of first microelectronic substrates to form a plurality of substrate assemblies;

for each substrate assembly, sequentially disposing portions of the conductive material to build up one of the conductive structures connected between the first and second connection sites of each substrate assembly; and

separating the substrate assemblies from each other.

[c25] 25. The method of claim 17 wherein coupling the first and second microelectronic substrates includes connecting the first and second microelectronic substrates to an intermediate structure.

[c26] 26. The method of claim 17 wherein disposing the conductive material includes disposing the conductive material to form an elongated conductive structure that extends in three orthogonal directions between the first and second connection sites.

[c27] 27. The method of claim 17 wherein disposing the conductive material includes disposing a non-self-supporting conductive material between the first and second connection sites.

[c28] 28. A method for packaging microelectronic substrates, comprising:

positioning a plurality of unsingulated first microelectronic substrates proximate to a corresponding plurality of singulated second microelectronic substrates while the first microelectronic substrates are connected to each other to form at least a portion of a microelectronic wafer, wherein each first microelectronic substrate has a first surface with a first connection site and further has a second surface facing opposite the first surface, and each second microelectronic substrate has a first surface with a second connection site and further has a second surface facing opposite the first surface;

attaching each second microelectronic substrate to a corresponding one of the plurality of first microelectronic substrates to form a plurality of substrate assemblies with the first surface of each first microelectronic substrate facing in at least approximately the same direction as the first surface of the corresponding second microelectronic substrate, and with the second surface of each

second microelectronic substrate facing toward the first surface of the corresponding first microelectronic substrate; and

for each substrate assembly, electrically connecting the first connection site of the first microelectronic substrate to the second connection site of the corresponding second microelectronic substrate with a conductive structure.

[c29] 29. The method of claim 28 wherein electrically connecting the first and second connection sites of each substrate assembly includes sequentially disposing at least first and second portions of a conductive material on the substrate assembly to build up the conductive structure.

[c30] 30. The method of claim 28 wherein electrically connecting the first and second connection sites of each substrate assembly includes conforming the conductive structure at least generally to a contour of the substrate assembly.

[c31] 31. The method of claim 28, further comprising for each substrate assembly:

disposing a first portion of dielectric material on the first microelectronic substrate;

disposing a second portion of dielectric material on the second microelectronic substrate; and

conforming the conductive material to the first and second portions of dielectric material.

[c32] 32. The method of claim 28, further comprising:

disposing a first portion of dielectric material on the first microelectronic substrate;

stacking the second microelectronic substrate on the first microelectronic substrate;

disposing a second portion of dielectric material on the second microelectronic substrate;

conforming a conductive material of the conductive structure to the first and second portions of dielectric material;

disposing a third portion of dielectric material on the conductive material;

coupling a third connection site to the conductive material with the third connection site electrically coupled to the first and second connection sites; and

disposing a volume of flowable conductive material on the third connection site to provide electrical communication with the first and second microelectronic substrates.

[c33] 33. The method of claim 28, further comprising positioning the first and second microelectronic substrates with the first and second connection sites facing in at least approximately the same direction.

[c34] 34. The method of claim 28, further comprising disposing a dielectric material on the first microelectronic substrate and conforming the conductive structure to a contour of the dielectric material.

[c35] 35. The method of claim 28 wherein disposing the conductive structure includes disposing the conductive structure to form an elongated conductive structure that extends in three orthogonal directions between the first and second connection sites.

[c36] 36. The method of claim 28 wherein disposing the conductive structure includes disposing a non-self-supporting conductive material between the first and second connection sites.

[c37] 37. A method for packaging microelectronic substrates, comprising:

positioning a plurality of unsingulated first microelectronic substrates proximate to a corresponding plurality of singulated second microelectronic substrates while the first microelectronic substrates are connected to each other to form at least a portion of a microelectronic wafer, wherein each first microelectronic substrate has a first surface with a first connection site and further has a second surface facing opposite the first surface, and each second microelectronic substrate has a first surface with a second connection site and further has a second surface facing opposite the first surface;

attaching each second microelectronic substrate to a corresponding one of the plurality of first microelectronic substrates to form a plurality of substrate assemblies with the first surface of each first microelectronic substrate facing in at least approximately the same direction as the first surface of the corresponding second microelectronic substrate, and with the second surface of each second microelectronic substrate facing toward the first surface of the corresponding first microelectronic substrate, and with the first and second connection sites facing in at least approximately the same direction; and

for each substrate assembly, electrically connecting the first connection site of the first microelectronic substrate to the second connection site of the corresponding second microelectronic substrate by sequentially disposing at least first and second portions of a conductive material on the substrate assembly to build up a conforming elongated conductive structure connected between the first and second connection sites, at least a portion of the conductive structure conforming at least generally to a contour of the substrate assembly.

[c38] 38. The method of claim 37, further comprising:

disposing a first portion of dielectric material on the first microelectronic substrate;

disposing a second portion of dielectric material on the second microelectronic substrate; and

conforming the conductive material to the first and second portions of dielectric material.

[c39] 39. The method of claim 37, further comprising:

disposing a first portion of dielectric material on the first microelectronic substrate;

stacking the second microelectronic substrate on the first microelectronic substrate;

disposing a second portion of dielectric material on the second microelectronic substrate;

conforming the conductive material to the first and second portions of dielectric material;

disposing a third portion of dielectric material on the conductive material;

coupling a third connection site to the conductive material with the third connection site electrically coupled to the first and second connection sites; and

disposing a volume of flowable conductive material on the third connection site to provide electrical communication with the first and second microelectronic substrates.

[c40] 40. The method of claim 37, further comprising disposing a dielectric material between the first surface of the first microelectronic substrate and the second surface of the second microelectronic substrate and coupling the first and second microelectronic substrates to each other by adhering the first and second microelectronic substrates to the dielectric material.

[c41] 41. A method for packaging microelectronic substrates, comprising:

positioning a first microelectronic substrate proximate to a second microelectronic substrate, the first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface, the second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface;

coupling the first and second microelectronic substrates to form a stacked substrate assembly with the first surface of the first microelectronic substrate facing toward the second surface of the second microelectronic substrate;

connecting the first connection site to the second connection site with a conductive connector; and

providing the assembly for connecting to other microelectronic devices while a planform area of the assembly in a plane generally parallel to the second surface of the first microelectronic substrate has a size and shape at least approximately identical to that of the second surface of the first microelectronic substrate.

[c42] 42. The method of claim 41 wherein coupling the first and second microelectronic substrates includes coupling the first and second microelectronic substrates with the first and second connection sites facing in generally the same direction.

[c43] 43. The method of claim 41 wherein the first microelectronic substrate has a planform area larger than a planform area of the second microelectronic substrate, and wherein providing the assembly for connecting to other microelectronic devices includes providing the assembly without disposing an

encapsulating material around an edge of the first microelectronic substrate between the first and second surfaces of the first microelectronic substrate.

[c44] 44. The method of claim 41, further comprising electrically coupling the substrate assembly to an external electronic device while an edge of the first microelectronic substrate between the first and second surfaces of the first microelectronic substrate is exposed.

[c45] 45. The method of claim 41 wherein connecting the first and second connection sites includes sequentially disposing at least first and second portions of a conductive material on the substrate assembly to build up a conforming elongated conductive structure connected between the first and second connection sites.

[c46] 46. A method for packaging microelectronic substrates, comprising:

positioning a first microelectronic substrate proximate to a second microelectronic substrate while the first microelectronic substrate forms at least a portion of a microelectronic wafer, the first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface, the second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface;

coupling the first and second microelectronic substrates to form a stacked substrate assembly with the first surface of the first microelectronic substrate facing toward the second surface of the second microelectronic substrate;

connecting the first connection site to the second connection site with a conductive connector;

singulating the first microelectronic substrate from other first microelectronic substrates of the microelectronic wafer after connecting the first connection site to the second connection site; and

electrically connecting the substrate assembly to other microelectronic devices while edges of the first microelectronic substrate between the first and second surfaces of the first microelectronic substrate remain exposed.

[c47] 47. The method of claim 46 wherein coupling the first and second microelectronic substrates includes coupling the first and second microelectronic substrates with the first and second connection sites facing in generally the same direction.

[c48] 48. The method of claim 46, further comprising electrically coupling the substrate assembly to an external electronic device while edge of the first microelectronic substrate between the first and second surfaces of the first microelectronic substrate is exposed.

[c49] 49. The method of claim 46 wherein connecting the first and second connection sites includes sequentially disposing at least first and second portions of a conductive material on the substrate assembly to build up a conforming elongated conductive structure connected between the first and second connection sites.

[c50] 50. A microelectronic device package, comprising:

a first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface;

a second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface, the second microelectronic substrate being coupled to the first microelectronic substrate to form a substrate assembly with the second surface of the second microelectronic substrate facing toward the first surface of the first microelectronic substrate; and

a conformal conductive link coupled between the first and second connection sites, the conductive link conforming at least generally to a contour of the substrate assembly immediately adjacent to the conformal conductive link.

[c51] 51. The package of claim 50 wherein the first and second connection sites face in at least approximately the same direction.

[c52] 52. The package of claim 50 wherein the conductive link conforms to a plane at least approximately parallel to the first surface of at least one of the first and second microelectronic substrates.

[c53] 53. The package of claim 50, further comprising:

a first portion of dielectric material disposed on the first microelectronic substrate; and

a second portion of dielectric material disposed on the second microelectronic substrate, wherein the conductive material conforms to the first and second portions of dielectric material.

[c54] 54. The package of claim 50, further comprising:

a first portion of dielectric material disposed on the first microelectronic substrate;

a second portion of dielectric material disposed on the second microelectronic substrate, wherein the conductive material conforms to the first and second portions of dielectric material;

a third portion of dielectric material disposed on the conductive material;

a third connection site coupled to the conductive material and the first and second connection sites; and

a volume of flowable conductive material disposed on the third connection site to provide electrical communication with the first and second microelectronic substrates.

[c55] 55. The package of claim 50 wherein the first microelectronic substrate has an exposed edge between the first and second surfaces.

[c56] 56. The package of claim 50, further comprising a dielectric material disposed on the first microelectronic substrate and wherein the conductive structure conforms to a contour of the dielectric material.

[c57] 57. The package of claim 50 wherein the first microelectronic substrate has a first planform area in the plane of the second surface of the first microelectronic substrate and wherein the second microelectronic substrate has a second planform area in the plane of the second surface of the second microelectronic substrate, with the second planform area less than the first planform area.

[c58] 58. The package of claim 50, further comprising a dielectric material disposed between the first surface of the first microelectronic substrate and the second surface of the second microelectronic substrate, the first and second microelectronic substrates being adhered to the dielectric material.

[c59] 59. The package of claim 50, further comprising an intermediate structure connected between the first and second microelectronic substrates.

[c60] 60. The package of claim 50, further comprising an adhesive film disposed between the first and second microelectronic substrates.

[c61] 61. The package of claim 50 wherein the conductive link includes an elongated conductive structure that extends in three orthogonal directions between the first and second connection sites.

[c62] 62. The package of claim 50 wherein the conductive link is non-self-supporting.

[c63] 63. The package of claim 50 wherein the first microelectronic substrate includes an SRAM device and the second microelectronic substrate includes a flash memory device.

[c64] 64. The package of claim 50 wherein the conductive link is a first conductive link, and wherein the package further comprises:

a third microelectronic substrate coupled to the second microelectronic substrate, the third microelectronic substrate having a first surface with a third connection site, the third microelectronic substrate further having a second surface facing opposite the first surface, the second surface of the third microelectronic substrate facing toward the first surface of second microelectronic substrate; and

sequentially disposed first and second portions of a second conductive link disposed on the substrate assembly and extending between the third connection site of the third microelectronic substrate and the second connection site of the second microelectronic substrate.

[c65] 65. A microelectronic device package, comprising:

a first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface;

a second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface, the second microelectronic substrate being coupled to the first microelectronic substrate with the second surface of the second microelectronic substrate facing toward the first surface of the first microelectronic substrate; and

a conductive link coupled between the first and second microelectronic substrates, the conductive link including a first portion of a conductive material disposed on at least one of the first and second connection sites, the conductive link further including a second portion of a conductive material sequentially disposed on the first portion to link the first connection site to the second connection site.

[c66] 66. The package of claim 65 wherein the conductive link conforms to at least one of the first microelectronic substrate and a dielectric material disposed on the first microelectronic substrate.

[c67] 67. The package of claim 65 wherein the conductive link conforms to a plane at least approximately parallel to the first surface of at least one of the first and second microelectronic substrates.

[c68] 68. The package of claim 65, further comprising:

a first portion of dielectric material disposed on the first microelectronic substrate;

a second portion of dielectric material disposed on the second microelectronic substrate, wherein the conductive material conforms to the first and second portions of dielectric material;

a third portion of dielectric material disposed on the conductive material;

a third connection site coupled to the conductive material and the first and second connection sites; and

a volume of flowable conductive material disposed on the third connection site to provide electrical communication with the first and second microelectronic substrates.

[c69] 69. The package of claim 65 wherein the first microelectronic substrate has an exposed edge between the first and second surfaces.

[c70] 70. The package of claim 65, further comprising a dielectric material disposed between the first surface of the first microelectronic substrate and the second surface of the second microelectronic substrate, the first and second microelectronic substrates being adhered to the dielectric material.

[c71] 71. The package of claim 65, further comprising an adhesive film disposed between the first and second microelectronic substrates.

[c72] 72. The package of claim 65 wherein the conductive link includes an elongated conductive structure that extends in three orthogonal directions between the first and second connection sites.

[c73] 73. The package of claim 65 wherein the conductive link is non-self-supporting.

[c74] 74. A microelectronic device assembly, comprising:

a wafer having a plurality of non-singulated first microelectronic substrates, each first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface;

a plurality of second microelectronic substrates each having a first surface with a second connection site and further having a second surface facing opposite the first surface, the second microelectronic substrates being coupled to the first microelectronic substrates while the first microelectronic substrates are non-singulated, and wherein the first surface of each first microelectronic substrate faces toward the second surface of a corresponding one of the plurality of second microelectronic substrates; and

a conductive link connected between the first and second connection sites.

[c75] 75. The assembly of claim 74 wherein the conductive link conforms to a contour defined by the coupled first and second microelectronic substrates.

[c76] 76. The assembly of claim 74 wherein the conductive link includes first and second sequentially deposited conductive portions.

[c77] 77. The package of claim 74 wherein the first and second connection sites face in at least approximately the same direction.

[c78] 78. The package of claim 74, further comprising:

a first portion of dielectric material disposed on the first microelectronic substrate;

a second portion of dielectric material disposed on the second microelectronic substrate, wherein the conductive material conforms to the first and second portions of the dielectric material;

a third portion of dielectric material disposed on the conductive material;

a third connection site coupled to the conductive material and the first and second connection sites; and

a volume of flowable conductive material disposed on the third connection site to provide electrical communication with the first and second microelectronic substrates.

[c79] 79. The package of claim 74 wherein the first microelectronic substrate has an exposed edge between the first and second surfaces.

[c80] 80. The package of claim 74, further comprising a dielectric material disposed between the first surface of the first microelectronic substrate and the second surface of the second microelectronic substrate, the first and second microelectronic substrates being adhered to the dielectric material.

[c81] 81. The package of claim 74, further comprising an adhesive film disposed between the first and second microelectronic substrates.

[c82] 82. The package of claim 74 wherein the conductive link includes an elongated conductive structure that extends in three orthogonal directions between the first and second connection sites.

[c83] 83. The package of claim 74 wherein the conductive link is non-self-supporting.

[c84] 84. A microelectronic device package, comprising:

a first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface;

a second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface, the first microelectronic substrate being attached to the second microelectronic substrate with the first surface of the first microelectronic substrate facing the second surface of the second microelectronic substrate and the first and second connection sites facing in at least approximately the same direction to define a microelectronic device assembly, wherein a planform area of the assembly in a plane generally parallel to the second surface of the first microelectronic substrate has a size and shape at least approximately identical to that of the second surface; and

a conductive link between the first and second connection sites.

[c85] 85. The package of claim 84 wherein the conductive link conforms to at least one of the first surface of the first microelectronic substrate and a material disposed on the first surface of the microelectronic substrate.

[c86] 86. The package of claim 84 wherein the first and second connection sites face in at least approximately the same direction.

[c87] 87. The package of claim 84, further comprising:

a first portion of dielectric material disposed on the first microelectronic substrate;

a second portion of dielectric material disposed on the second microelectronic substrate, wherein the conductive material conforms to the first and second portions of dielectric material;

a third portion of dielectric material disposed on the conductive material;

a third connection site coupled to the conductive material and the first and second connection sites; and

a volume of flowable conductive material disposed on the third connection site to provide electrical communication with the first and second microelectronic substrates.

[c88] 88. The package of claim 84 wherein the first microelectronic substrate has an exposed edge between the first and second surfaces, and wherein the package further comprises a microelectronic device external to the assembly and electrically coupled to the assembly while the edge is exposed.

[c89] 89. The package of claim 84, further comprising a dielectric material disposed between the first surface of the first microelectronic substrate and the second surface of the second microelectronic substrate, the first and second microelectronic substrates being adhered to the dielectric material.

[c90] 90. The package of claim 84, further comprising an adhesive film disposed between the first and second microelectronic substrates.

[c91] 91. The package of claim 84 wherein the conductive link includes an elongated conductive structure that extends in three orthogonal directions between the first and second connection sites.

[c92] 92. The package of claim 84 wherein the conductive link is non-self-supporting.

[c93] 93. An electronic device, comprising:

a housing; and

a microelectronic device package positioned within the housing, the microelectronic device package including:

a first microelectronic substrate having a first surface with a first connection site and further having a second surface facing opposite the first surface;

a second microelectronic substrate having a first surface with a second connection site and further having a second surface facing opposite the first surface, the second microelectronic substrate being coupled to the first microelectronic substrate to form a substrate assembly with the second surface of the second microelectronic substrate facing toward the first surface of the first microelectronic substrate; and

a conformal conductive link coupled between the first and second connection sites, the conductive link conforming at least generally to a contour of the substrate assembly.

[c94] 94. The device of claim 93 wherein the conductive link includes first and second portions of sequentially deposited conductive material.

[c95] 95. The device of claim 93 wherein the packaged microelectronic device forms at least a part of a processor.

[c96] 96. The device of claim 93 wherein the packaged microelectronic device forms at least a part of a memory.